David Sarnoff Research Center
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CERAMIC/METAL COMPOSITE CIRCUIT-BOARD-LEVEL TECHNOLOGY FOR APPLICATION SPECIFIC ELECTRONIC MODULES (ASEMs)

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TECHNICAL REPORT

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March 13, 1995

Advanced Research Projects Agency
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Attention: Electronic Systems Tech Office
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Subject: Contract DAAB07-94-C-C009
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(9/22/94-3/14/95)

Gentlemen:

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Date: 3/13/95

Certifying Official: Barry Thaler

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Summary

During this final quarter of the Phase 1 program, high density test structures were fabricated to demonstrate that LTCC-M is a robust circuit board technology. Reliability tests were performed on all elements of the 2-sided multilayer structure. During this past year all major elements of the LTCC-M technology have been developed and demonstrated. These developments are listed below:

Phase 1 Developments

Features	Developed
Low Cost Feedthrough Process	✓
• Hole fabrication with laser	✓
• Hole insulation	✓
• Center conductor	✓
Green Tape Development	✓
• Glass/ceramic	✓
• Low loss ceramic	✓
• Low CTE ceramic	✓
• Green tape formulation	✓
Ceramic to Metal Bonding	✓
• Cu/Mo/Cu surface preparation	✓
• Glaze development	✓
• "Zero" lateral shrinkage	✓
Conductor Development	✓
• Buried silver conductor	✓
• Via silver conductor	✓
• Top AgPd conductor	✓
• Top Au conductor	✓
Multilayer Integration	✓
• Double-sided board fabrication and firing	✓
Thin Film Process	✓
• Thin film conductors on glass/ceramic	✓
• BCB processing	✓
• Thin film multilayers on LTCC-M	✓

During this period LTCC-M passed all reliability tests on the different elements of the multilayer structure. These tests are summarized below:

Reliability Tests on Different Elements of the Multilayer Structure

- Feedthrough Integrity: 25 thermal shocks(-77 to +150°C) with no degradation
- Ceramic to metal adhesion: 300 cycles(-40 to +125°C) with no degradation
- Ceramic Hermeticity: >1600 hours HHBT(85/85, 48v) with no silver migration
- 1-sided ceramic multilayer: >250 cycles with no degradation or cracking
- 2-sided ceramic multilayer + feedthroughs: >90 cycles with no degradation or cracking
- Cyclotene™ with conductors on multilayer ceramic: 100 cycles with no degradation, cracking, or delamination

Section I
WBS Task 1.1: Metal Core Fabrication

A. TASK OBJECTIVE

The metal core fabrication serves 2 distinct purposes in the manufacture of double sided low temperature cofired ceramic on metal (LTCC-M) substrates. These are: (1) to provide a high density of electrical interconnections between the top and bottom sides of the substrate, and (2) to restrain the shrinkage of the ceramic during firing, so that **"zero" lateral shrinkage** is achieved Within this task are 2 entirely separate developments; namely (1) the development of materials and processes to fabricate many small electrical feedthroughs within the metal core and (2) the development of materials and processes to fire the ceramic onto the metal core with "zero" x-y shrinkage.

B. INTRODUCTION

In previous technical reports the feedthrough fabrication process was described and verified with machine drilled holes (0.013" diameter). The basic feedthrough fabrication process involves opening up a hole (e.g. drilling and deburring), applying a layer of nickel to seal the molybdenum, depositing an annular ring of insulation, and finally depositing a conductor in the center core of the insulator. The insulation and center conductors are deposited by modified screen printing techniques, using standard equipment. This process has been extended to laser drilled holes as small as 7 mils in diameter. Laser drilling has been identified as the fastest and most cost-effective method for drilling a large number of small holes in a metal core. Additional data has been collected on laser drilled holes this past quarter.

C. ELECTRICAL FEEDTHROUGH FABRICATION RESULTS

Two new vendors for laser drilling 13 mil diameter holes in the Cu/Mo/Cu metal core were developed this past quarter. They are Chromalloy Research & Technology (Orangeburg, NY) and Applied Laser Technology (Beaverton, OR). Chromalloy Research & Technology employed a Nd:YAG laser, while Applied Laser Technology drilled the holes with a YAG laser. In both cases the amount of "slag" residue remaining around the perimeter of the holes was significantly reduced below the amount produced last quarter by Coherent General. However, removal by mechanical means was still required. Removing the slag by forming a small chamfer on the outer lip of the holes (both sides) is the recommended method, since this also aids the flow of the insulating glass into the hole in subsequent process steps.

Feedthroughs were fabricated using laser drilled holes having chamfers. These feedthroughs were then subjected to the same thermal shock test (-77°C to +150°C) as the mechanically drilled holes. After 25 thermal shock cycles, the feedthroughs did not exhibit any degradation, nor were any cracks observed in the surrounding ceramic insulation.

D. SHRINKAGE CONTROL

The key property of the LTCC-M process that sets it apart from all other cofired ceramic technologies is the simple method used to restrain the ceramic from shrinking in the lateral plane, while obtaining a fully sintered ceramic. This is accomplished by the use of a custom glass bonding layer that attaches the ceramic to the metal core during the ceramic firing process. Additionally, the ceramic has good adhesion to metal core. The development of a the bonding layer seems to be quite specific to the green tape formulation.

This past quarter it was shown the bonding technology described in the last quarterly report can be directly carried over to the ABT-36 series of ceramic compositions. The adhesion of the ABT-36 ceramic to the Cu/Mo/Cu metal core was measured by a pull test on an Instron Universal Testing Machine. Precut 7 mm squares of ABT-36 (4 layers thick) were colaminated onto the Cu/Mo/Cu core that was prepared for bonding. The average pull strength for 15 samples was 17.14 ± 5.6lbs; this converts to a pull strength of about 250 lbs/in^2, a very high strength for a glass to metal seal. Thermal cycling (-40°C to +125°C) similarly prepared parts does not cause any degradation of the bond strength of this interface. These results will be presented in the reliability section of this report. this indicates very good compatibility between the Cu/Mo/Cu metal core, the ABT-36 series green tape, and the LTCC-M bonding process.

E. PLAN FOR NEXT QUARTER

- This task has been completed and all requirements met.

Section II
WBS Task 1.2: LTCC Ceramic Development

A. TASK OBJECTIVE

The development of glass-ceramic dielectric compositions suitable for the fabrication of LTCC-M on Cu/Mo/Cu cores and having high density, thick film silver wiring.

B. INTRODUCTION

The development of glass-ceramic dielectric compositions suitable for the fabrication of LTCC-M on Cu/Mo/Cu cores and having high density, thick film silver wiring. The specific requirements for the glass are the following:

(i). The glass should densify and crystallize in the temperature range of 850° - 950°C.

(ii) In the sintered and crystallized state, its coefficient of thermal expansion should closely match that of Cu/Mo/Cu from room temperature to the sintering temperature range

(iii) The glass should be strong, non-porous, and resist silver migration.

(iv) The glass-ceramic should possess a low dielectric constant for use in high speed digital packaging applications

(v) The glass-ceramic should also possess very low values for dissipation factor at microwave frequencies for use in high frequency communication packaging applications.

(vi) The glass-ceramic should be resistant to etching in chemicals commonly used in plating nickel and gold.

(viii) It is preferred that the glass composition not contain any lead.

We had reported earlier on the development of glasses in the forsterite composition field of the $MgO\text{-}Al_2O_3.SiO_2$ system, in particular a glass designated as KU-4, which was found to posses substantially all of the required attributes for this application. Then, in the last report, we had discussed the need to modify the KU-4 composition to more closely match the CTE to that of Cu/Mo/Cu cores, as well as to lower sintering temperature somewhat. These had been successfully accomplished through the additions of a seeding additive and a fluxing glass to obtain a ceramic composition that was designated as ABT-24. This composition enabled us to obtain flat-firing LTCC-M substrates on Cu/Mo/Cu cores for the first time. The silver ink compositions for buried lines were developed using this composition. However, ABT-24 was found to have higher dielectric loss values in GHz range than desired and, the fluxing additive used was lead-based. In this reporting period we have successfully modified the original KU-4 dielectric composition once again to obtain a lead-free dielectric glass-ceramic that is well suited for LTCC-M fabrication of Cu/Mo/Cu.

C: MODIFICATION OF GLASS-CERAMIC DIELECTRIC:

The new glass composition is designated as KU-14. Nearly 12 batches of KU-14 glass have been prepared to date and have been characterized by DTA and other means. The ceramic composition for the tape , now designated as ABT-36

series contains small amounts (0.1 - 2 %) of a reactive filler to enhance crystallization. The role of this filler is to ensure that abundant nucleation of the crystalline phases occurs during the glass sintering and that the crystallization occurs to completion throughout the body of the ceramic at reasonable temperatures. The DTAs of KU-14 glass alone and when admixed with the filler material are shown in Figure II.1. The figure shows a lowering of nearly 15°C in the peak crystallization temperature, as well as more pronounced crystallization in the presence of the additive

The silver inks for buried lines, originally formulated for ABT-24, could be used with ABT-38 without modification. However, via inks and top surface inks had to be reformulated. This reformulation was successfully Cu/Mo/Cu out during this last reporting period. The peak firing temperature for ABT-36 green tape series is 900°-925°C.

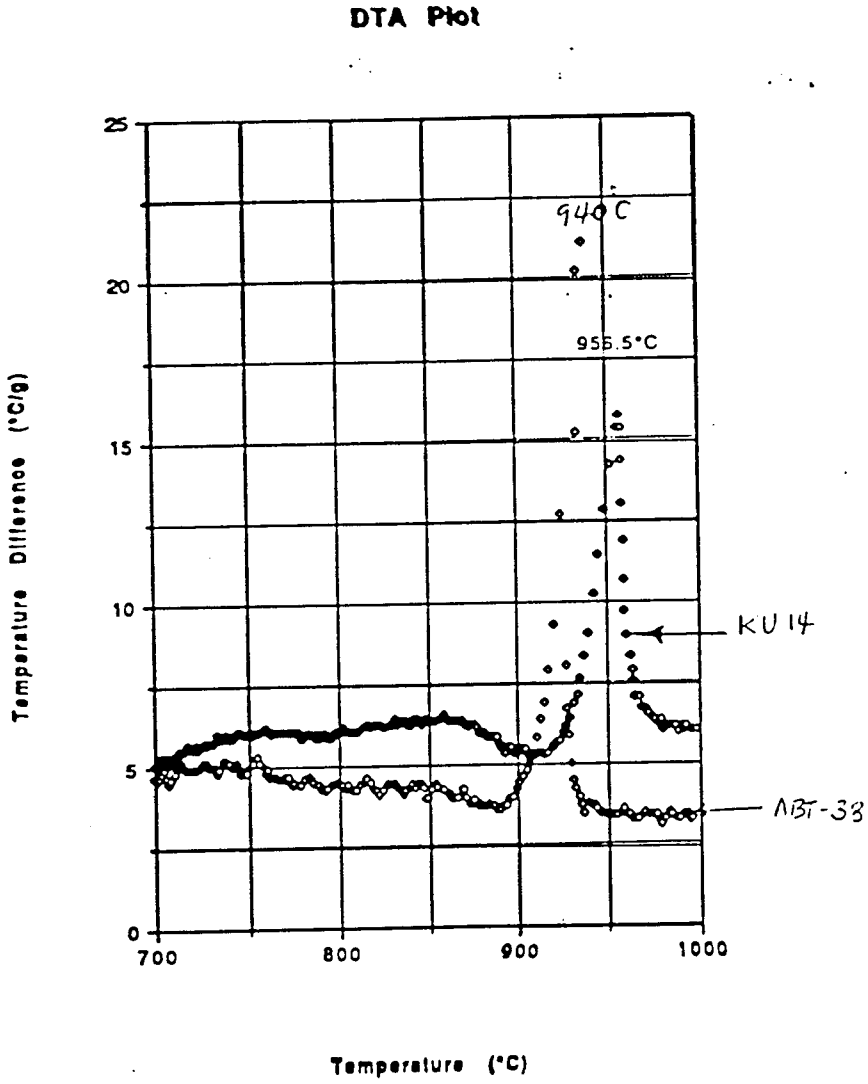

Figure II.1: DTA plot showing the effect of the reactive filler on the crystallization of KU-14 glass.

The ABT-36 dielectric composition has been successfully used to fabricate many LTCC-M structures on Cu/Mo/Cu cores, including all of the reliability test vehicles built during this period using the methods described earlier. Some of these substrates contained silver conductors and thin film interconnect structures. In all cases the substrates exhibited little or no camber or other processing problems. The fired dielectric composition has also been found to be easily polished to very high surface smoothness suitable for high density thin film interconnect fabrication. The microstructure of the fired dielectric shows a two phase structure with very little porosity.

The dielectric properties of ABT-38 (one of the ABT-36 series green tape formulations) glass-ceramic are as follows

Peak Firing Temperature (°C)	900	910
Dielectric Constant	5.77	5.63
Dielectric Loss (tanδ) at 15 GHz	0.0034	0.0018

X-ray diffraction of the sintered glass-ceramic indicated that the glass-ceramic is comprised of nearly equal amounts of a-cordierite ($Mg_2Al_4Si_5O_8$) and forsterite (Mg_2SiO_4) crystalline phases with small amounts of enstatite ($MgSiO_3$) and residual glass making up the remainder.

D. FUTURE WORK

This concludes the development work on ceramic dielectric for this phase of the ASEM contract. A dielectric composition well suited for LTCC-M fabrication on Cu/Mo/Cu and, having characteristics required for digital and microwave packaging applications, has now been developed. Detailed documentation for glass preparation, including grades and sources of raw materials, melting practice, milling methods, tape slurry preparation etc. exists in our records, to form the basis of technology transfer planned for the next program phase. A commercial vendor for the dielectric glass has been identified and the first batch of glass is being procured for qualification evaluations.

Section III
WBS Task 1.3: Cofired Conductors

A. TASK OBJECTIVE

The objective of this task is to develop silver thick film conductor inks capable of producing high density circuits. This will include the development of a buried conductor, a via-fill conductor, and a top conductor. These conductors will subjected to the relevant reliability tests.

B. INTRODUCTION

To fabricate multilayer cofired ceramic interconnect boards, three conductors, having different requirements, must be developed for the ABT-36 green tape. The conductors in the buried layers are required to have high electrical conductivity and fine line printing characteristics. The vias connecting the different layers of the circuit must be hermetic to insure the long term reliability of the circuit. The top layer conductor must solderable, plateable, and have good adhesion to the glass-ceramic.

C. BURIED CONDUCTOR

It was determined that ABT-36 green tape was compatible with silver thick film ink formulations containing no glass at all. It is expected that the elimination of glass will produce conductors having the highest electrical conductivity. The measured resistivity of thick film conductors printed and fired as buried conductors in ABT-36 green tape is 3-4 mΩ/square.

D. VIA CONDUCTOR

Via conductor inks are formulated by mixing silver powder (from Degussa) with glass and an organic vehicle (to obtain the desired rheology for stencil printing). To prevent separation (or cracking) of the silver via from the surrounding glass-ceramic, via formulations generally have a higher glass content than conductor trace inks. The via inks have been significantly improved compared to those reported in the last quarterly report. For ABT-36 green tape, a high softening point glass from the KU-4 glass family has been incorporated into the via formulation. Figure III.1 shows the DTA characteristics of this glass. Test structures with 8 mil diameter vias show good compatibility between the via formulation and the buried and top conductor inks. Daisy chain test structures having 80-120 8 mil diameter vias/chain are consistent with a via resistivity of 5-10 mΩ/layer.

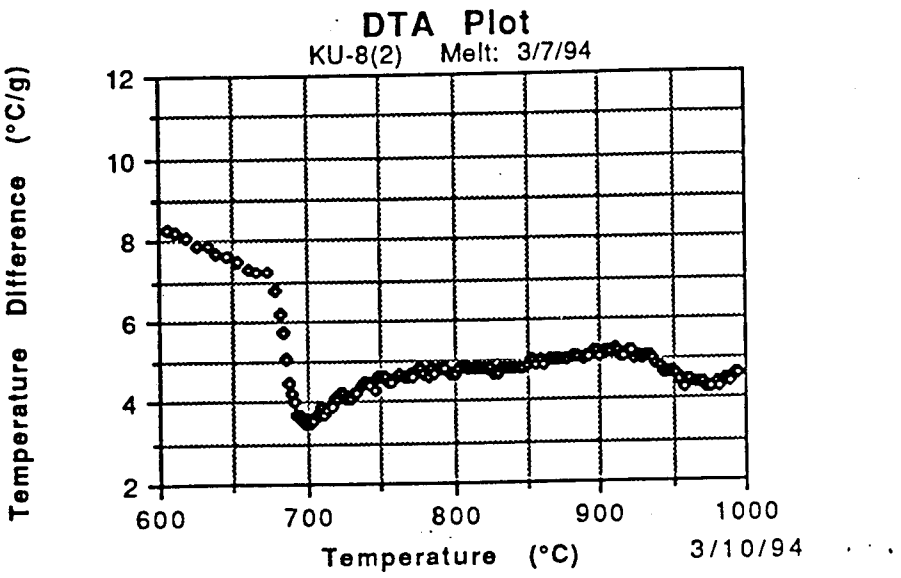

Figure III.1 : DTA of the custom glass KU-8 added to the via formulation

E. TOP CONDUCTOR INKS

A Ag ink formulation containing a low softening point PbO glass has been found acceptable as cofired top conductor. These conductors can then be plated with Ni/Au for reliability. The plated conductors are solderable and wirebondable with Au or Al wire.

A AgPd (30 wt%Pd) ink formulation containing a high softening point glass has exhibited good adhesion to the ABT-36 ceramic after cofiring. This conductor can then have AgPd ink postfired onto it for good solderability.

A Au ink formulation containing a low softening PbO glass has been found acceptable as a postfired to conductor for wirebonding pads.

F. PLAN FOR NEXT QUARTER

- This task has been completed.
- Adapt ink rheology to merchant manufacturer during the technology transfer portion of the Phase 2 program.

Section IV
WBS Task 1.4: Thin Film Interconnect Structures

A. TASK OBJECTIVE

The objective of this part of the program is to demonstrate that MCM-D interconnect structures can be built on top of the ASEM ceramic substrate. This will be accomplished by the actual fabrication of a multi-level, thin film interconnect structure on the final ASEM test vehicle and subjecting this structure to the relevant reliability tests.

B. INTRODUCTION

In this the last reporting period of Phase 1, our specific objectives were to fabricate dense thin film interconnect structures to permit the evaluation of substrate factors that might influence processing and yields, and the reliability of such structures, including the electrical integrity of the thick film silver-to - thin film interfaces.

C. THIN FILM PROCESS:

i) Thin film process selection:

We had reported earlier on the evaluation several different thin film processes and dielectric materials to fulfill the objectives of this task. After the initial evaluations, we had narrowed the choice of thin film dielectric's to two types of benzo-cyclo-butene (BCB) supplied by Dow Chemical Company. The photo-sensitive version of BCB would simplify the thin film fabrication process because the material functions both as a photoresist and as a permanent dielectric. Nevertheless, we chose to work with the non-photo-sensitive BCB (Cyclotene™) because certain processing issues such as the reliable exposure and development method for fine (10-25 μm diameter) would have needed significant optimization.

(ii) Thin Film Process:

The following processing sequence was used for thin film interconnect fabrication. The description of individual process steps, which varies from tool to tool, is on record.

(a) Capture pad and first -level metal definition

1. Sputter Ti-Cu seed layer (1500Å Cu)
2. Apply photoresist, Expose 1st. level of thin film, and develop
3. Electroplate Copper (5 μm) through resist openings
4. Remove resist
5. Remove TiCu seed layer by ion milling

(b) Via definition

6. Spin Apply adhesion promoter and Cyclotene™ 3022-57
7. Cure in flowing nitrogen at 250°C for 1 hour
8. Sputter 2000Å Cu as a mask

9. Apply photoresist, expose via pattern and develop
10. Wet etch copper ($FeCl_3$) through exposed resist to define via mask
11. Plasma Etch vias in Cyclotene™
12. Strip Cu mask in $FeCl_3$

(c) Top metal:

13. Sputter TiCu seed for top metal
14. Apply photoresist, expose top metal pattern and develop resist
15. Electroplate top metal Cu-Ni-Au
16. Remove seed layer of Ti-Cu by ion-beam milling

(iii) Substrate attributes :

The LTCC-M substrates with ABT-36 dielectric were found to easy to polish to very high surface finish (~150Å CLA) to obtain nearly pore-free surface for thin film fabrication. The camber of the substrates was low so that the planarization during polishing could be contained within one layer (0.004") of ceramic on the 2.5" x 2.5" parts. The glass-laden silver vias were found to be well adhered to the ceramic walls, and showed no cracking, separation, pits etc. in the polished parts. The nickel-plated Cu/Mo/Cu cores held up well to thermal processing steps in the process. There was some concern regarding the differential heating of the metal core in plasma ashers and etchers used in the process. It is felt these concerns can be alleviated by ashing in the so-called down-stream ashers where the sample is exposed to the plasma outside the RF field.

(iv) Thin Film Test Structures:

Two types of thin film test structures were designed, to match up with two types of ceramic test vehicles that were built to evaluate reliability. Both these test vehicles, consisted of two levels of thin film wiring, one level right on the polished ceramic surface and another on top of the BCB dielectric layer. Vias of 25, 50 and 75 μm diameters interconnected the thin film wiring in the two levels. The structure was also interspersed with fully testable, dense thin film wiring (thin film lines of 25 μm lines/50 μm pitch, 50 μm lines/100 μm pitch), to obtain an estimate of interconnect yields.

Another aspect of the test vehicles was that they yielded many fully testable via daisy chains consisting of thick film silver lines in the ceramic, thick film via to thin film capture pad interfaces, and thin film wiring on two levels of the structure. These were electrically characterized initially and after temperature cycling for yield and reliability assessments. The results, discussed in another part of this report, showed that the thin film innocents can be fabricated on the LTCC-M substrates at high yields, and that these structures were highly reliable.

D. PLAN FOR NEXT QUARTER

- This task has been completed.

Section V
WBS Task 1.5: Multilayer Integration

A. TASK OBJECTIVE

This task integrates together the metal core with feedthroughs, the green tape, all thick film conductors, and the "zero" shrinkage processing to fabricate double-sided test substrates. This will verify the compatibility of all the processes, which were individually developed in WBS Tasks 1.1 to 1.4.

B. INTRODUCTION

The previous sections described the development of materials and processes for the major components of the double-sided LTCC-M structure. This section will describe the results of their integration into high density daisy chain test structures.

C. MULTILAYER INTEGRATION RESULTS

This past quarter a daisy chain test structure was designed to test the LTCC-M fabrication processes developed during this Phase 1 contract. The structures fabricated from this pattern are designed to individually test the major elements of the structure shown in Figure V.1.

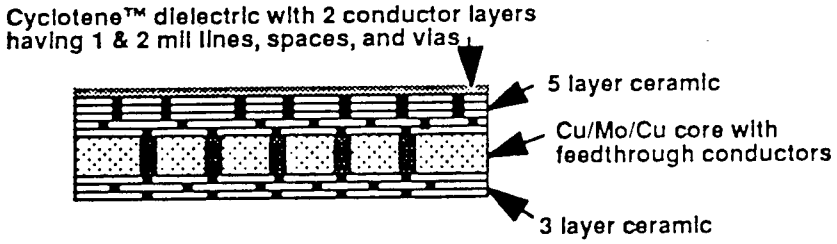

Figure V.1: High density test structure fabricated to demonstrate the integrity of the LTCC-M materials system.

1-sided Test Structures

The initial structures to be fabricated used this pattern as 1-sided test boards having 4 interconnected LTCC-M layers, without the Cyclotene™ thin film overlay. The general daisy chain structure (all layers combined) is shown in Figure V.2. This figure shows that 9 chains are produced from each sample. The daisy chains demonstrate high, medium, and low density structures in the LTCC-M circuit board. Some details of the pattern are shown in Table V.1.

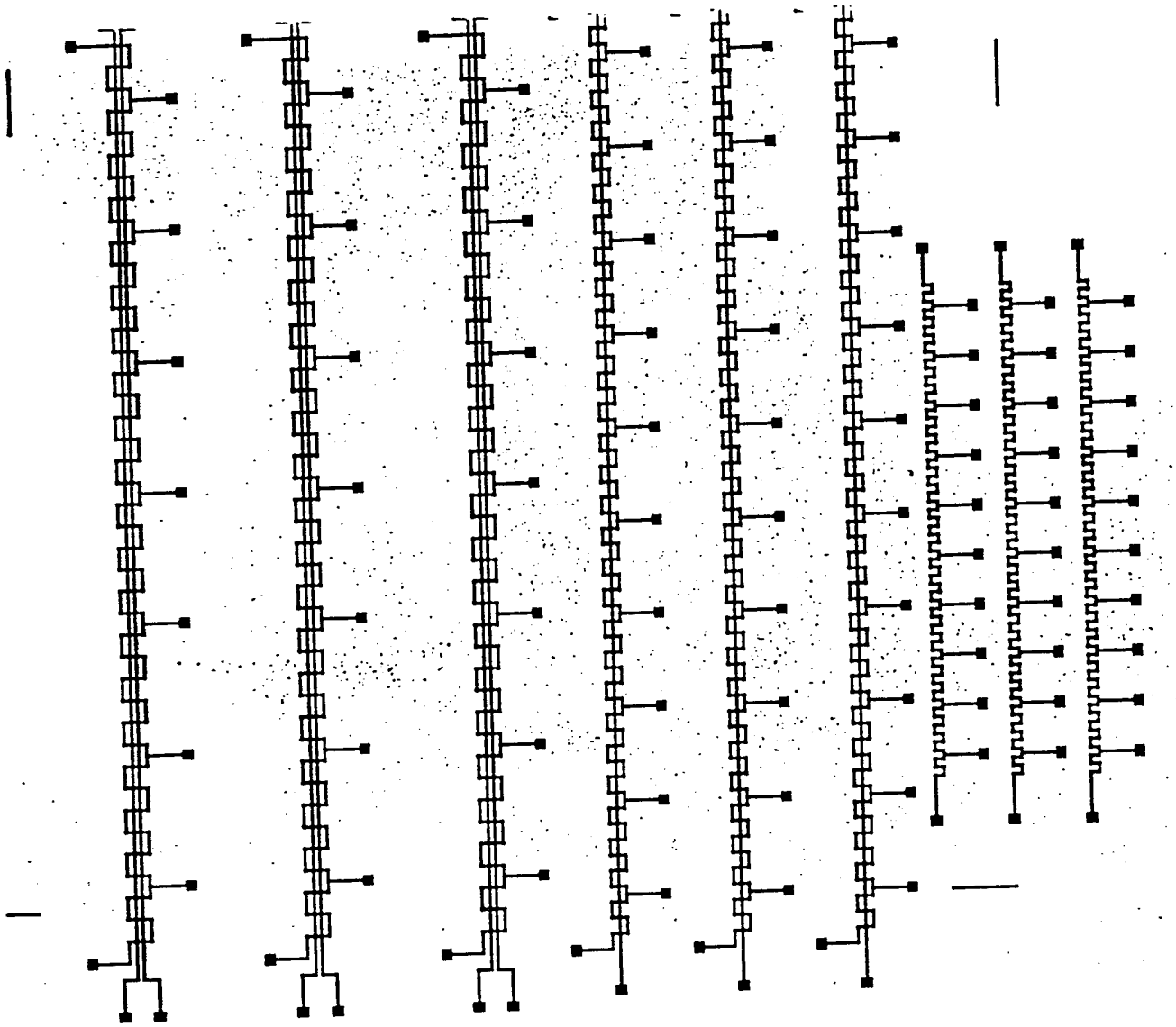

Figure V.2: Composite of all 4 thick film layers of the LTCC-M high density daisy chain pattern.

Layout Statistics
1-sided Test Structures

- 4 layer daisy chain pattern
- 9 daisy chains interconnecting a total 978 vias
- High density via region:
  - No lines between vias
  - 8 mil diameter vias on 16 mil centers
  - 120 vias/chain
- Medium density region:
  - 8 mil vias on 30 mil centers
  - Allows 1 circuit trace line (8 mil line/7 mil space) between vias
  - 120 vias/chain
- Low density region:
  - 8 mil vias on 42 mil centers
  - Allows 2 circuit trace lines (8 mil line/6 mil space) between vias
  - 84 vias/chain

Table V.1

These 1-sided test structures were successfully fabricated using the conductor designs shown in Figures V.3 - V.6. After fabrication these test structures were subjected to thermal cycle (-40°C to + 125°C) testing and did not exhibit any degradation.

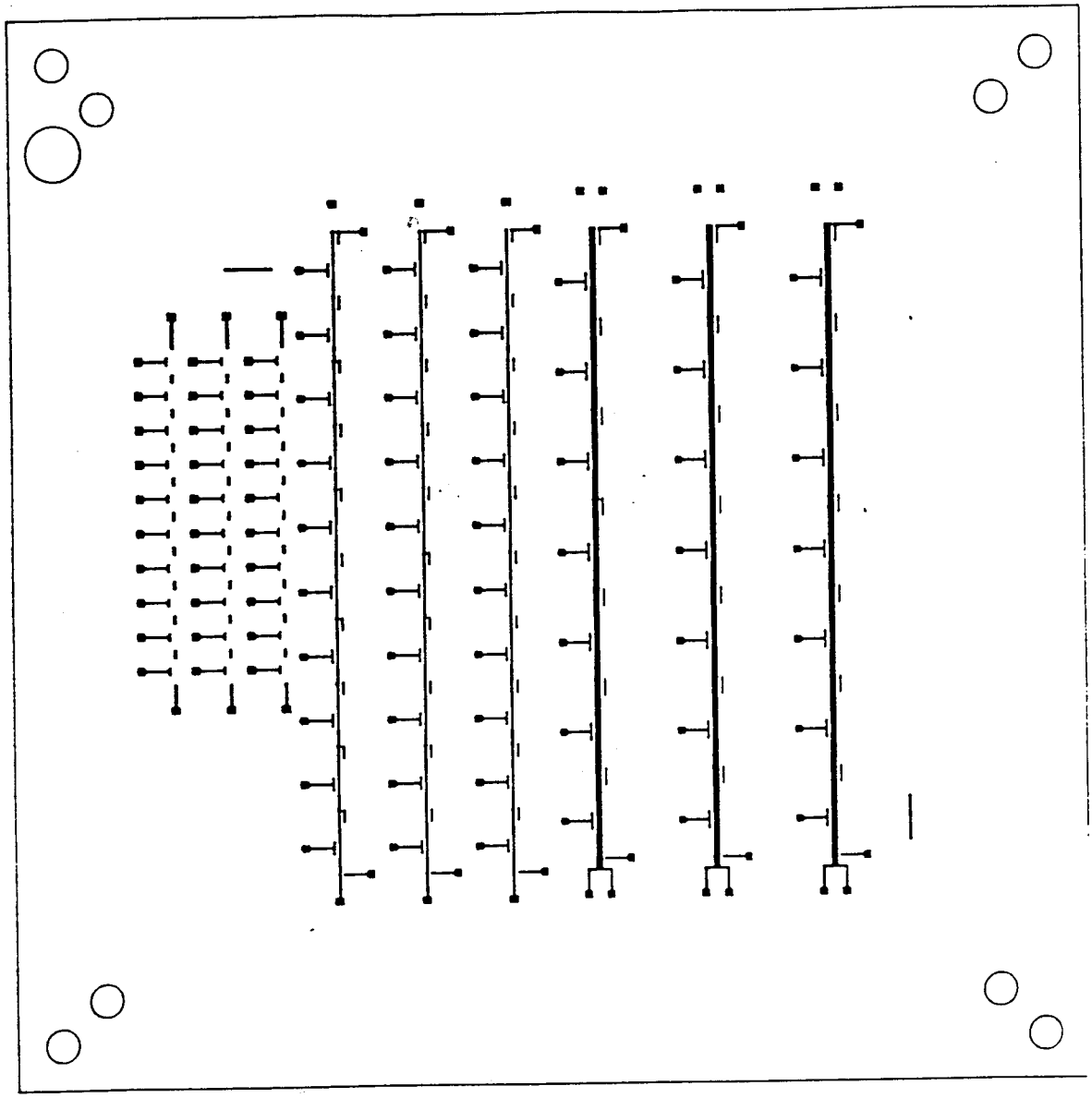

Figure V.3: **Top layer (layer#1) conductor pattern for the high density daisy chain pattern.**

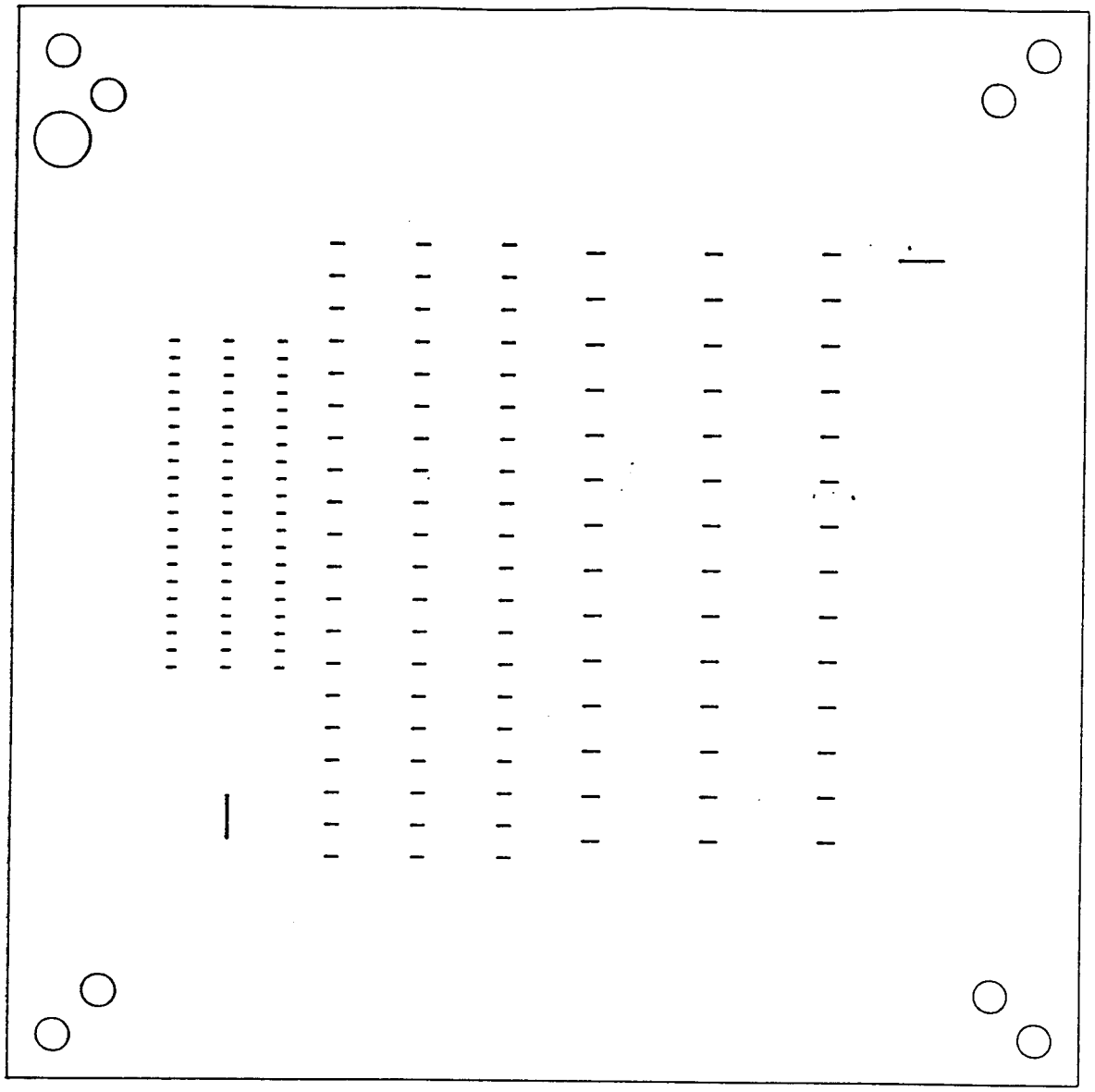

Figure V.4: Layer#2 conductor pattern for the high density daisy chain pattern.

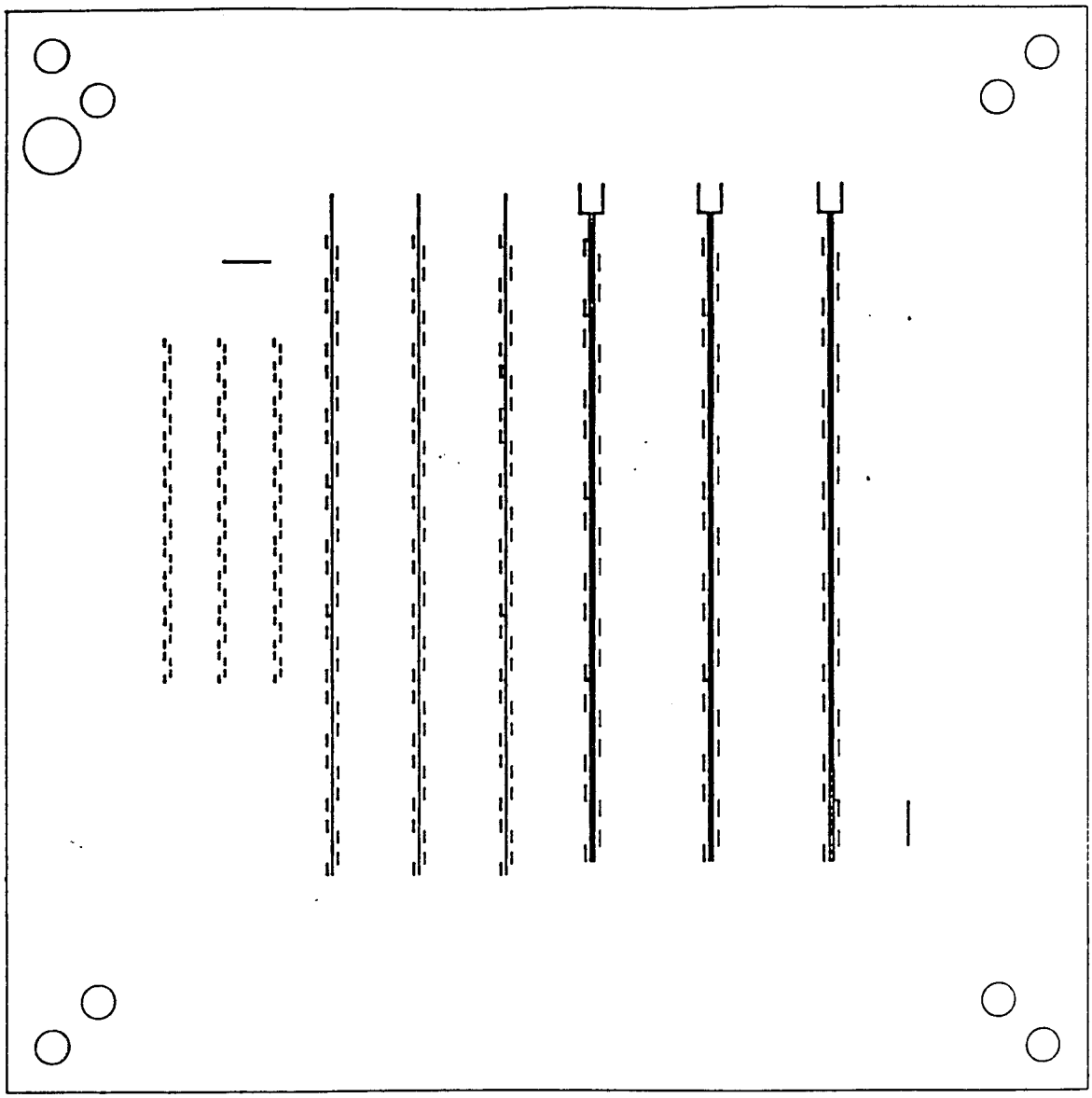

Figure V.5: Layer#3 conductor pattern for the high density daisy chain pattern.

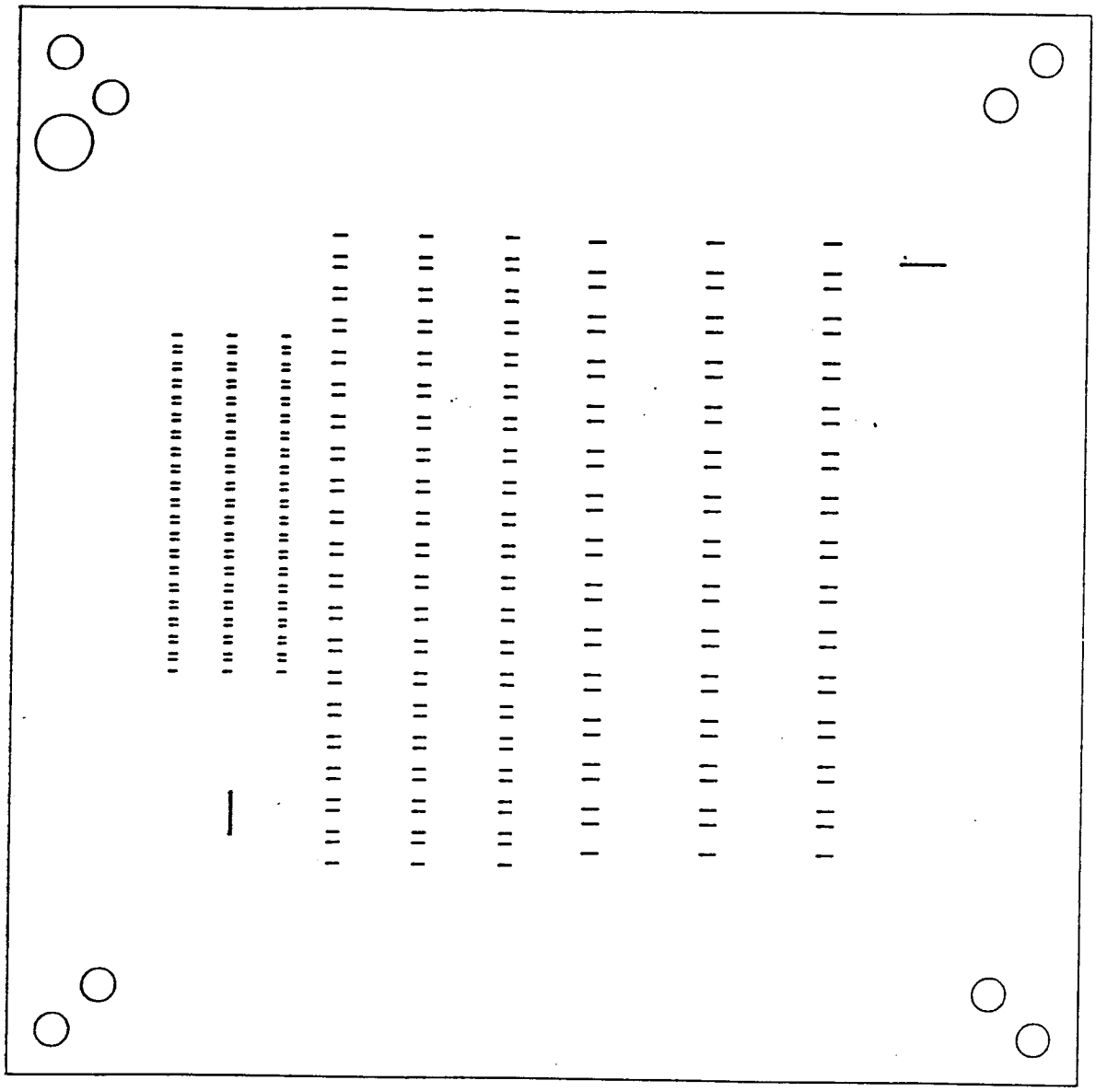

Figure V.6: **Bottom layer (layer#4) conductor pattern for the high density daisy chain pattern.**

2-sided Test Structures

Next, 2-sided test structures were fabricated on a metal core having electrical feedthroughs using the same basic test pattern. However, the top of the board had three layers (layers #1-3), and the bottom of the board had the fourth layer (and 2 additional layers for handling integrity). The electrical feedthroughs in the Cu/Mo/Cu core connected layer #3 on the topside to layer #4 on the bottomside. The electrical feedthroughs were mechanically drilled, which limits their density to only connect the medium and low density areas of the test pattern. Therefore, only 6 daisy chains are interconnected on the 2-sided test structures. The details of the 2-sided test structures without thin film overlays are shown below in Table V.2.

Layout Statistics
2-sided Test Structure (LTCC-M only)

- 4 layer daisy chain pattern
- Cu/Mo/Cu has 204 13 mil diameter electrical feedthroughs
- 6 daisy chains interconnecting a total 822 vias in the ceramic
- Medium density region:
  - 8 mil vias on 30 mil centers
  - Allows 1 circuit trace line (8 mil line/7 mil space) between vias
  - 120 vias + 40 feedthroughs/chain
- Low density region:
  - 8 mil vias on 42 mil centers
  - Allows 2 circuit trace lines (8 mil line/6 mil space) between vias
  - 84 vias + 28 feedthroughs/chain

Table V.2

These 2-sided test structures were successfully fabricated using the conductor designs similar to those shown in Figures V.3 - V.6. After fabrication these test structures were subjected to thermal cycle (-40°C to + 125°C) testing and did not exhibit any degradation.

Low Density Test Structures with thin film BCB polymer overlays

A 36 hole/layer (a 6 x 6 matrix of 8 mil vias on 200 mil centers) test pattern was initially used to develop the processing for adding BCB polymer overlays to LTCC-M ceramic circuits. The test structures were 1-sided circuit boards fabricated with 4 layers of interconnected vias in the ceramic, and 2 conductor layers of thin film conductors connected together in daisy chain fashion. One of the thin film patterns test is shown in Figure V.7. The details of these test structures are shown below in Table V.3.

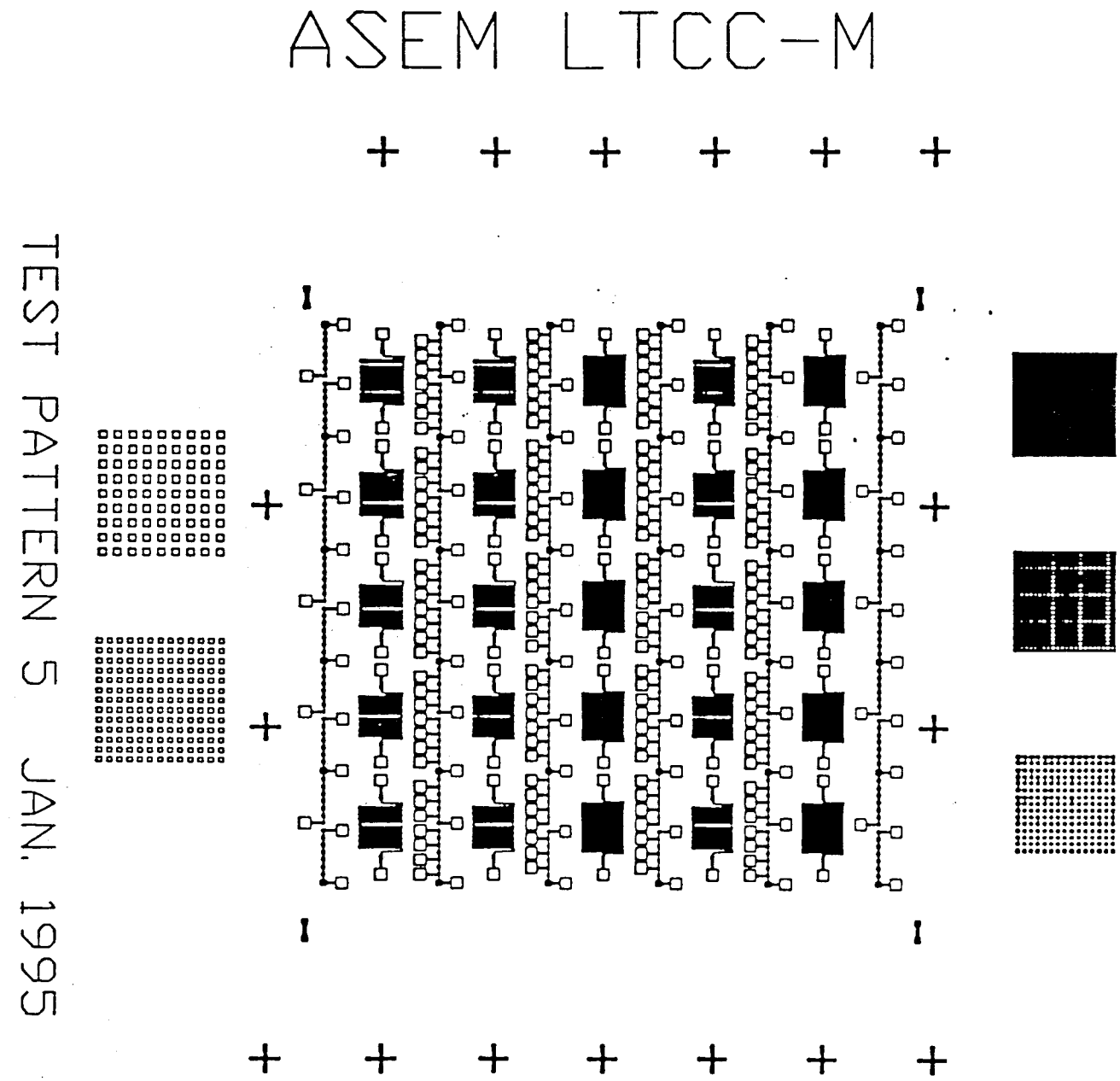

Figure V.7: Low density thin film test pattern for LTCC-M

Layout Statistics
low density pattern with BCB overlay

- 2 level BCB daisy chain
  - 1 and 2 mil lines, spaces, and vias
  - 3 mil diameter capture vias to ceramic vias
  - 508 thin film vias
  - 25 1 and 2 mil wide meander line patterns
- 4 layers of LTCC-M
- 6 chains interconnecting a total 108 vias in the ceramic

Table V.3

These 1-sided test structures with thin film conductors were successfully fabricated. After fabrication these test structures were subjected to thermal cycle (-40°C to + 125°C) testing and did not exhibit significant degradation.

2-sided High Density Test Structures with thin film BCB polymer overlays

The test structures schematically shown in Figure V.1 were fabricated using the general test pattern shown in Figures V.2 - V.5. However, the top layer (layer #1) conductor pattern was replaced with a 2 layer thin film conductor daisy chain pattern. This 2-sided pattern consists 5 layers on the top side of the metal core (2 sacrificial layers for polishing) and 3 layers on the bottom side. The thin film pattern is deposited on the top side after polishing. The design of the conductors (both layers shown together) is shown in Figure V.8. The details of this design are shown in Table V.4. This test pattern was successfully fabricated with a very low level of defects.

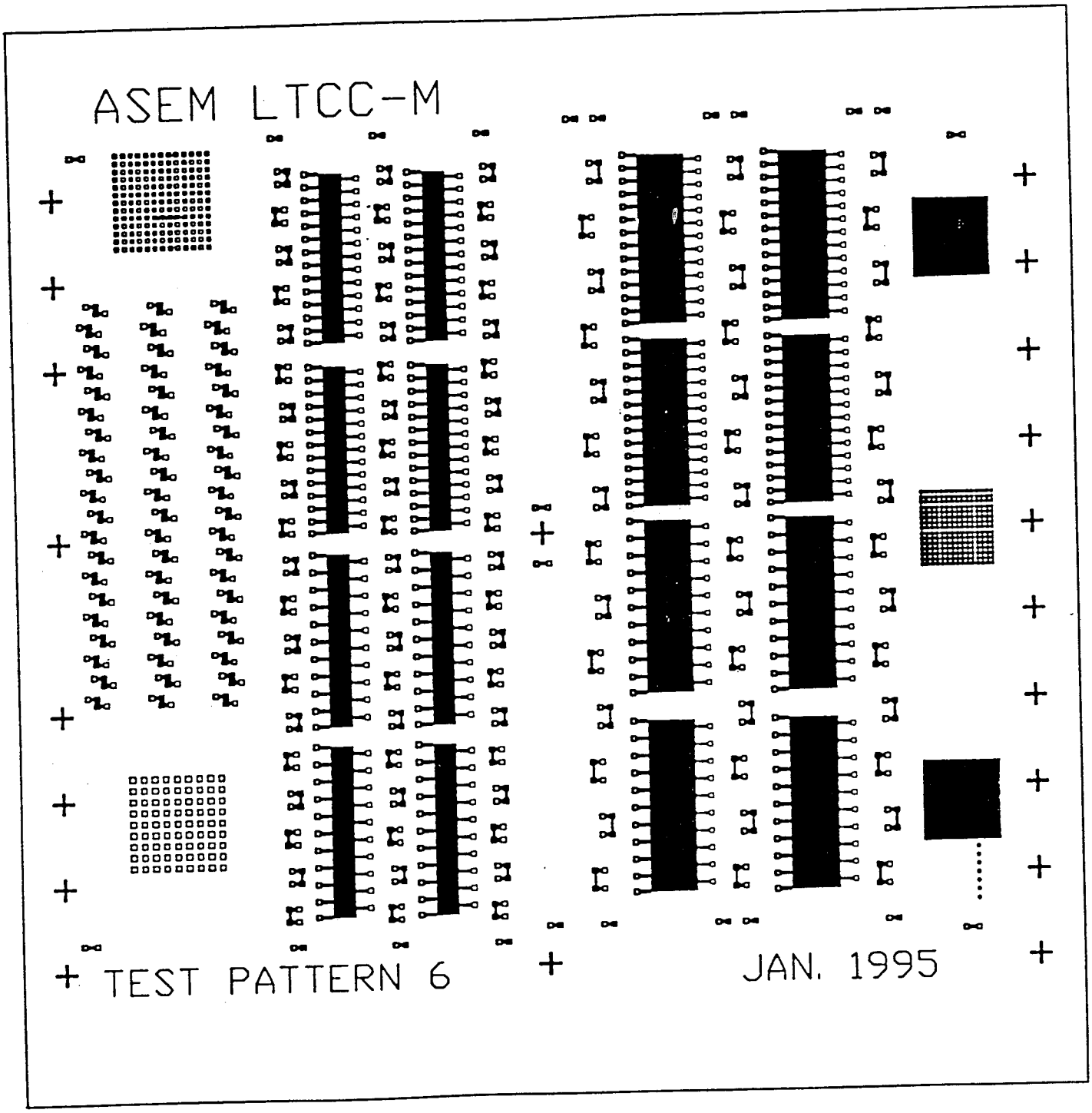

Figure V.8: High density thin film test pattern for LTCC-M

Layout Statistics
2-sided LTCC-M with BCB Overlay

- 2 level BCB daisy chain
  - 1 and 2 mil lines, spaces, and vias
  - 3 mil diameter capture vias to ceramic vias
  - 987 vias
  - 16 meander line patterns
- 8 layers of LTCC-M (total)
- Cu/Mo/Cu has 204 13 mil diameter electrical feedthroughs
- 6 daisy chains interconnecting a total 1242 vias in the ceramic

Table V.4

D. PLAN FOR NEXT QUARTER

- This task has been completed.
- Use the 1 and 2-sided test structure designs to demonstrate the technology transfer of the LTCC-M circuit board process to the merchant manufacturer during the Phase 2 program.

Section VI
WBS Task 1.5: Reliability Studies

A. TASK OBJECTIVE

This tasks will verify the compatibility of all the processes, which were combined in the Multilayer Integration task (WBS Tasks 1.5). The integrated test structures described in the previous section will be subjected to thermal cycling and high humidity bias and temperature (HHBT) accelerated aging tests.

B. INTRODUCTION

The principal reliability failure tests of multilayer ceramic substrates are to induce failures by thermal cycling stresses or by silver migration. Thermal cycling stresses cause cracking and/or open circuits. Silver migration leads to "short circuits" and is tested by HHBT tests.

C. SILVER MIGRATION TESTING

The silver migration test pattern consists of a parallel plate capacitor structure having 1 layer of green tape ceramic as the dielectric, a thick film silver buried electrode, and a thick film AgPd (30% Pd) top electrode. The test is performed in a temperature humidity chamber set for a constant temperature and humidity of 85°C and 85%RH. The voltage across the capacitor structure is 48 volts, with the top electrode negative relative to the buried electrode. Tests were run on 1-sided ABT-36 samples (4 layer samples) with the silver migration capacitors formed around the top ceramic layer.

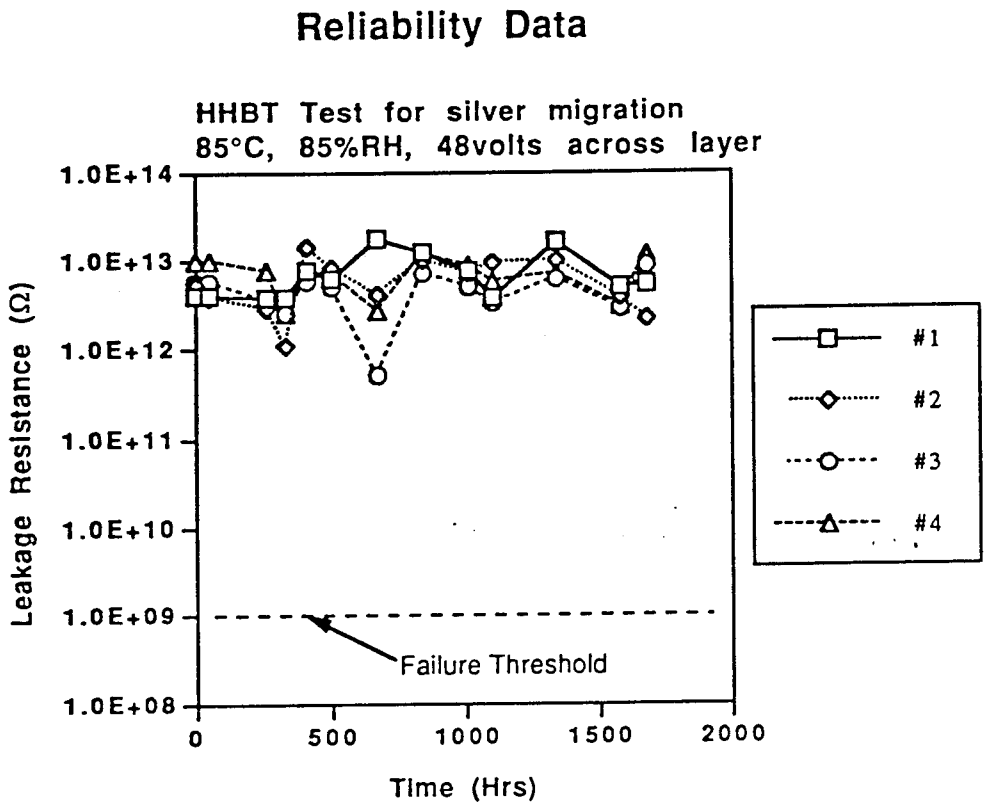

Figure VI.1: HHBT Test results show that the low porosity of the ABT-36 LTCC-M resists silver migration.

As can be in Figure VI.1, silver migration failures are not observed in the ABT-36 ceramic. This verifies that this ceramic sinters to a very high density during firing, which will prevent reliability problems due to silver migration.

D. THERMAL CYCLING TESTS

The thermal cycle employed in all of the tests described in this report is between -40°C and +125°C, with a 30 minute dwell at each temperature. The temperature ramped up to 125°C in 1 hour, and ramped down to -40°C in 2 hours.

1-sided Test Structures

The results of the thermal cycling tests on 1-sided high density test structures are shown in Figure VI.2.

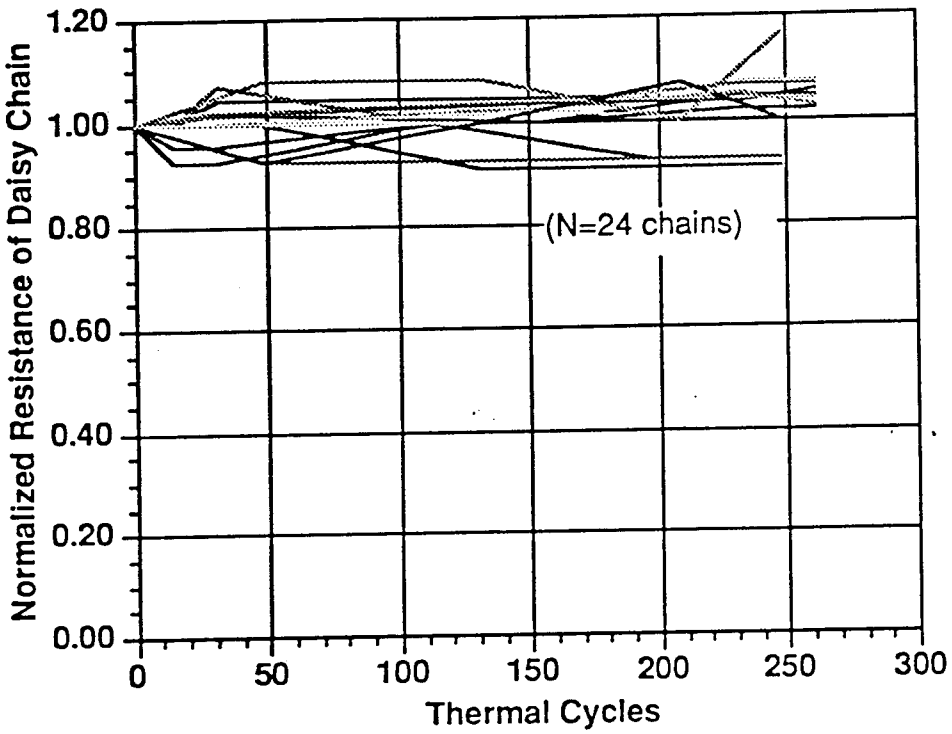

Figure VI.2: Thermal Cycling results for 1-sided high density test pattern samples show no degradation.

Figure VI.2 shows that the resistance of each daisy chain remains constant throughout the test period. Additionally, observation using a low power microscope (40X) did not reveal any cracking caused by the thermal cycle stresses. This indicates very good compatibility between the LTCC-M ceramic and the thick film vias.

2-sided Test Structures

The results of thermal cycling of 2-sided test structures (without thin film overlays) is shown in Figure VI.3.

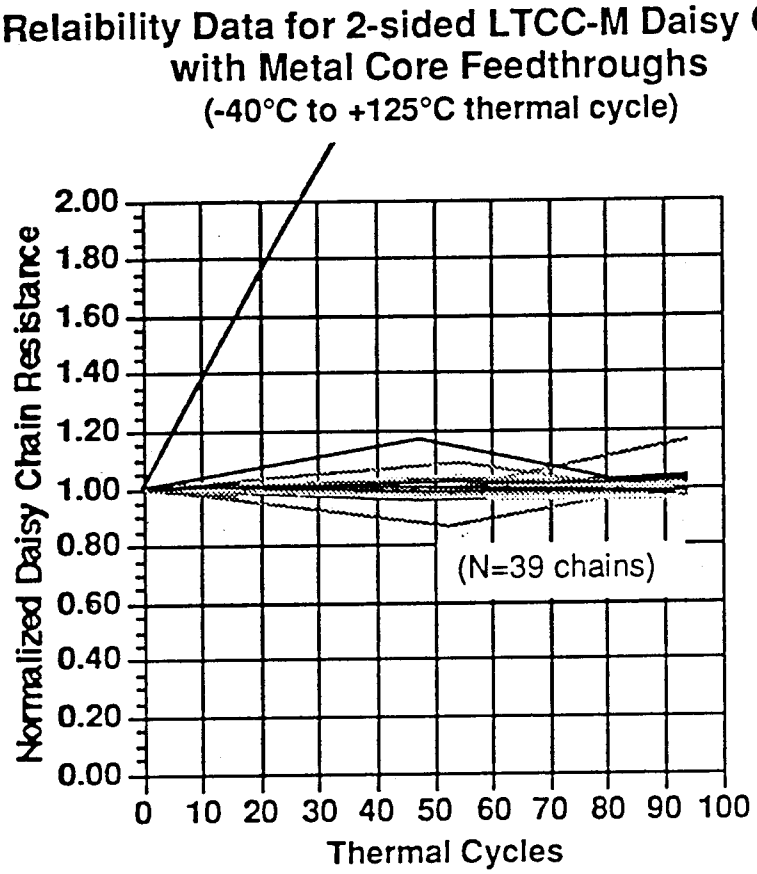

Figure VI.3: Thermal Cycling results for 2-sided high density test pattern samples show no degradation.

Figure VI.3 shows that the resistance of the daisy chains for 2-sided LTCC-M samples having electrical feedthroughs remains constant. Of the thousands of vias and feedthroughs tested, one daisy chain link ever failed. The fact that it failed very shortly after testing began, suggests that this was a marginal connection, and is not indicative the robust vias and feedthroughs that are produced by the LTCC-M process. Additionally, examination of the circuit boards with a low power microscope did not reveal any cracking of the vias. These results point to the good compatibility among all of the LTCC-M components.

Low Density Test Structures with thin film BCB polymer overlays

About 60 thin film daisy chains (4 vias/chain) in BCB overlays on LTCC-M ceramic were subjected to 100 thermal cycles. The adhesion of the BCB polymer to the polished ceramic remained acceptable (it could not be removed by the scotch tape test) after 100 thermal cycles. Only 3 chains exhibited failure during this time. These failures started to appear early in the test (<24 cycles). Since all of these failures occurred in the same area of a single test sample, these failures are initially attributed to incomplete opening up of the via in the BCB dielectric by the plasma etch step. The fact that the vast majority (95%) of the daisy chains tested showed a constant resistance, indicates good compatibility between the LTCC-M ceramic and BCB polymer overlays.

An additional group of samples (150 daisy chains) having longer thin film daisy chains (8 or 15 vias/chain) have been tested through 24-42 cycles. Their results also show a constant daisy chain resistance, and are in complete agreement with samples that have been cycled 100 times.

Ceramic to Metal Adhesion

The adhesion of the ABT-36 ceramic to the Cu/Mo/Cu metal core was measured by a pull test on an Instron Universal Testing Machine. Precut 7 mm squares of ABT-36 (4 layers thick) were colaminated onto the Cu/Mo/Cu core that was prepared for bonding. Prior to conducting the pull test, samples were stored in the thermal cycling chamber. As shown in Figure VI.4, the adhesion of the LTCC-M ceramic to the Cu/Mo/Cu metal core is not significantly affected by storage in the thermal cycling chamber for 300 cycles. This is a further indication of the excellent compatibility between the bonding process, the LTCC-M ceramic, and the metal core.

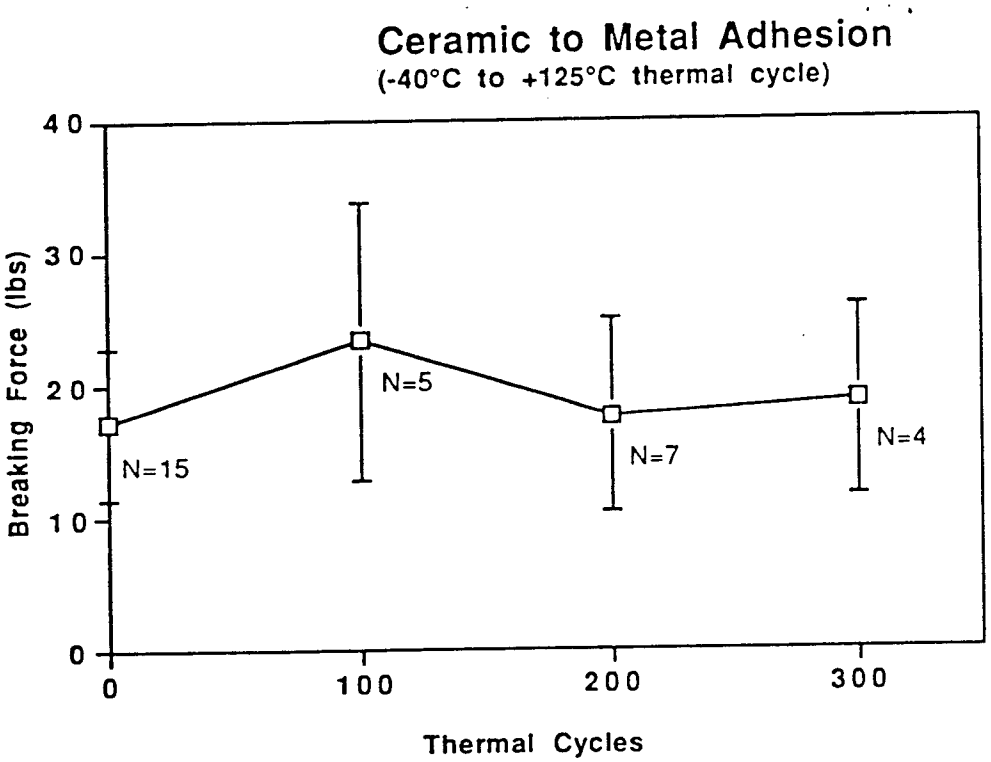

Figure VI.4: Thermal cycling does not produce any significant change in the adhesion of the LTCC-M ceramic to the metal core.

E. PLAN FOR NEXT QUARTER

- This task has been completed. The LTCC-M ceramic has passed all reliability tests.

Section VII
Important Findings

A. METAL CORE FABRICATION

- Two new vendors have successfully laser drilled in the Cu/Mo/Cu core.
- Electrical feedthroughs made from laser drilled holes have passed thermal shock testing (-77°C to +150°C)

B. LTCC-M CERAMIC DEVELOPMENT

- The green tape ceramic composition has been modified to provide low loss (0.001) at microwave frequencies (15 GHz)

C. COFIRED CONDUCTORS

- Developed a Ag via thick film ink formulation that shows excellent compatibility with the ABT-36 series of green tape formulations
- Developed a Ag top conductor that can be cofired with the green tape, and then is compatible with Ni/Au plating processes
- Developed a cofired AgPd (30% Pd) thick film ink that can be cofired with the green tape
- Developed a AgPd (30% Pd) thick film ink that can be postfired onto the glass-ceramic to provide a surface with good solderability
- Developed a Au thick film ink that can be postfired onto the glass-ceramic to provide a wirebondable surface

D. THIN FILM INTERCONNECT STRUCTURES

- Fabricated high density interconnects on top of 2-sided LTCC-M ceramic boards using Cyclotene™ (BCB) polymer

E. MULTILAYER INTEGRATION

- Fabricated high density LTCC-M ceramic circuit boards using 2-sided processing with a Cu/Mo/Cu metal core having large number of electrical feedthroughs

F. RELIABILITY STUDIES

The LTCC-M system passed all reliability tests as follows:

- Showed that the ceramic is very dense and will prevent silver migration under HHBT Testing (85°C, 85% RH, 48 volts) for more than 1600 hours.
- Showed that the vias and the ceramic are compatible through thermal cycling (-40°C to +125°C) for more than 250 cycles without any cracks developing or via failures.
- Showed compatibility of Cu/Mo/Cu metal core, bonding process and the glass-ceramic through 300 thermal cycles without any decrease in the ceramic to metal adhesion value.

- Showed that the LTCC-M system is compatible through thermal cycling of 2-sided high density test structures for more than 90 cycles without any cracks developing or significant electrical failures.
- Showed that Cyclotene™ (BCB) polymer overlays are compatible with LTCC-M circuit boards by thermal cycling test structures up to 100 cycles without any cracking, significant loss of adhesion to the ceramic, or significant electrical failures.

Section VIII
Significant Developments

The ABT-36 series of green tape was independently evaluated by Martin Marietta (Government Electronic Systems) for dielectric loss at microwave frequencies. Fired samples having a thin film conductor (Cr-Cu covered with a thin layer of Au) meander line pattern were supplied to Martin Marietta. The results showed a very low loss at microwave frequencies, that is acceptable for use in T/R modules.

Section IX
Plan for Further Research

This report completes the Phase 1 portion of this contract. The Phase 2 program will begin by concentrating on transferring the LTCC -M technology to a merchant circuit board supplier. Additionally, Phase 2 will validate the LTCC-M technology by fabricating a number of prototype modules. During the next quarter designs and layouts will be generated for fabrication of these modules using LTCC-M.

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The quarterly progress for the Ceramic/Metal Composite Circuit-Board-Level Technology for Application Specific Electronic Modules is described in this report. Data is reported for the following tasks: Metal Core Fabrication, LTCC Ceramic Development, Thin Film Interconnect Structure Integration, Multilayer Integration, and Reliability Studies.

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